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EXAMINER
MAI, ANH D

ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)
	09/392,034	GONZALEZ ET AL
	Examin r	Art Unit
	Anh D. Mai	2814

-- The MAILING DATE of this communication appears on th c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27,31-40,42 and 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27,31-40,42 and 43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 2, 2003 has been entered.

Amendment

2. Amendment filed January 2, 2003 has been entered as Paper No. 23. Claims 1, 3 and 4 have been amended. Claims 1-27, 31-40, 42 and 43 are pending.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "forming said liner upon side sidewall of said isolation trench comprises deposition of a composition of matter" (claim 4) and "removing the pad oxide and forming a gate oxide" (claim 8) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 2 and 34 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to

cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim 2 recites: "further comprising forming a liner upon a sidewall of each said isolation trench".

This limitation have been recited in claim 1.

Claim 34 recites: "a layer composed of polysilicon upon said gate oxide" (line 6).

The correct term is "a layer composed of polysilicon upon said oxide layer".

Note that, there is only one layer of polysilicon 24 formed on the substrate 12 and that layer 24 is formed on the pad oxide 14. (see Fig. #B).

Response to Amendment

5. The amendment filed **February 14, 2002** is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "said depositing is carried out to the extent of leaving no gap in each said isolation trench" and "said planarizing is performed in the absence of masking the conformal layer over each said isolation trench" and "liner being confined within each said isolation trench".

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1-27, 31-40, 42 and 43 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which **was not described in the specification** in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a **written description** of the claim limitation "depositing is carried out to the extent of **leaving no gap** in each said isolation trench" in the application as filed.

The specification as originally filed, fails to provide support for such a deposition.

Further, there does not appear to be a **written description** of the claim limitation "planarizing is performed **in the absence** of masking the conformal layer over each said isolation trench" in the application as filed. The same had been rejected in the previous Office Action.

7. Claims 4, 16 and 21 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for "**rounding the top edge of the trench**" by thermally grown oxide from the substrate, does not reasonably provide enablement for *rounding the top edge of trench* by **depositing material** on the trench surface. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

The specification clearly indicated that the rounding of the edge at the top of the isolation trench is a result of thermal oxidizing of the sidewall 50 to form the insulation liner 30. (See page 12, 1st paragraph). Further, as an alternative, the insulation liner can be formed by CVD.

Note that, rounding of the corner is a result of thermal oxidation, forming thermal liner. When the insulation liner forms by CVD, the CVD is deposited on the etched trench which have not been rounded by the oxidation. Therefore, depositing the insulation liner by CVD does not result in rounding the corner and rounding the corner is not formed by CVD.

The specification ***fails to provide support*** for rounding the top edge of the trench by depositing material (CVD).

It is well known in the semiconductor technology that by consuming silicon at the corner during the thermal oxidation, the top edge of the trench becomes rounded.

Deposition, e.g. CVD, on the other hand, **does not consume any material** from the silicon substrate. Therefore, rounding does not occur.

How can the edge of trench be rounded when no silicon is consumed ? (See Wolf).

8. Claims 14-17 and 21-23 are further rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for forming a thermal liner oxide 30 to be confined within each isolation trench, but does not reasonably provide enablement for depositing CVD, the liner 30 to be confined within each isolation trench. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

How can a dielectric material only be deposited within the trench ?

Regarding the formation of CVD on the substrate, see Omid-Zohoor '108, Fig. 3I, oxide liner (58b).

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-26 and 31-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

What is the limitation "wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches" (claims 1, 7, 14, 18, 24, 25, 26 and 31) or "wherein electrically insulative material extends continuously between and within said plurality of isolation trenches" (claim 35 and 38) referring to ?

The "material and electrically insulative material" **lacking antecedent**, thus making the claims indefinite.

What is "material that is electrically insulative extends continuously between and within the plurality of isolation trenches" referring to ?

The "material that is electrically insulative" have not been recited anywhere before.

Claim 13 recites: "wherein said ratio in a range from about 1.3:1 to about 1.7:1".

However, neither claim 7 nor claim 11, which claim 13 depends on, recite "a ratio".

10. Claims 9, 10, 12, 13, 26, 27, 29 and 30 recites the limitation, as an example claim 9, "wherein said upper surface for each said isolation trench is formed in an etch process using an etch recipe that etches said *first dielectric layer (nitride) faster than said conformal layer(oxide) and said spacers* (oxide) by a ratio in range from of about 1:1 to about 2:1" in lines 1-4. There is insufficient antecedent basis for this limitation in the claim.

However, the specification discloses the opposite, etch the oxide faster than the nitride layer. (See page 14, lines 14-25).

11. Claims 21-23 are further rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 21 recites the limitation "wherein said conformal third layer is composed of an electrically **conductive** material" in lines 5-6. There is insufficient antecedent basis for this limitation in the claim. (See Amendment D, filed February 14, 2002)

The conformal third layer as disclosed in the specification is "isolation film 36" and "spacer 28 and isolation film 36 are made from the same material" and the material used to form the spacer 28 is dielectric material (TEOS). Thus, this layer does not appear to be electrically conductive material, but rather electrically insulative material. (See specification and other claims).

12. Claims 21-23 are furthermore rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claims

21-23 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in the specification and claim 18, which claim 21 depends upon. In which, applicant has stated that the microelectronic structure is "**isolation trench**", and this statement indicates that the invention is different from what is defined in the claim(s) because to form an isolation trench, the trench fill material, e.g. conformal third layer should be electrically insulative material. Therefore, the limitation of claims 21-23 are in direct conflict with the invention "wherein said conformal third layer is composed of an electrically **conductive** material".

13. Claims 1-27, 31-40, 42 and 43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

These claims recite either: "said depositing is carried out to the extent of leaving no gap in each said isolation trench" or "said planarizing is performed in the absence of masking the conformal layer over each said isolation trench"

Claims 1-27, 31-40, 42 and 43 are indefinite because: they attempt to claim the invention by excluding what the inventor did not invent rather than distinctly and particularly pointing out what they did invent. *In re Schechter,* 205 F.2d 185, 98 USPQ 144 (CCPA 1953); MPEP 2173.05(i).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

14. Claims **1**-4, 6-13, **18**, 19, 21-27 and are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor et al. (U.S. Patent No. 6,097,072) in view of Omid-Zohoor et al. (U.S. Patent No. 6,184,108) (all cited previously).

With respect to claim 1 and 14, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) upon the oxide layer (340);

selectively removing the first dielectric layer (344) to exposed the oxide layer (340) at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer (340) and the first dielectric layer (344), wherein the forming the second dielectric layer (352) includes forming a second dielectric layer (352) over and in contact with the exposed oxide layer (340) at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer (352), wherein each spacer is situated upon the oxide layer (340), is in contact with the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer (340) into the semiconductor substrate (120), wherein each the isolation trench (360) is adjacent to and below the pair of the spacers (356) and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench (360) has a top edge;

filling each isolation trench (360) with a conformal layer (364), the conformal layer extending above the oxide layer (340) in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal layer (364), and the depositing is carried out to the extend of leaving no gap in each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344); and

planarizing the conformal layer (364) and each spacer (356) to form therefrom an upper surface for each isolation trench (376) that is co-planar to the other upper surfaces, wherein the planarizing is performed in the absence of masking the conformal layer over the isolation trench;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 2-3Q).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of forming a thermal liner upon the sidewall and rounding the top edge of the isolation trench (360).

However, Omid-Zohoor '108 teaches that it is well known in the art to form a thermal liner (58a) on the etched trench surface to remove damage caused by the trench-etch.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trench liner on the surface of trench (360) of Omid-Zohoor '072 as taught by Omid-Zohoor '108 to remove the damage caused by the trench-etch. Further, the growing of the thermal liner is **inherently** resulted in rounding the top corner of the trench.

With respect to claims 2 and 3, as best understood by the examiner, the liner (58a) of Omid-Zohoor '108 is formed upon the sidewall of each isolation trench and is a thermally grown oxide of the semiconductor substrate .

With respect to claim 4, as best understood by the examiner, liner (58b) of Omid-Zohoor '108 comprises deposition of a composition of matter.

With respect to claim 6, as best understood by the examiner, the upper surface for each isolation trench (376) of Omid-Zohoor is formed by CMP.

With respect to claim 7, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a first dielectric layer (344) upon the oxide layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer (340) at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer (340) and the first dielectric layer (344);

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer (356) is situated upon the oxide layer (340), is in contact with the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer (340) into the semiconductor substrate (120), wherein each the isolation trench is adjacent to and below the pair of the spacers (356) and is situated at the corresponding area of the plurality of areas;

filling each the isolation trench with a conformal layer (364), the conformal layer extending above the oxide layer (340) in contact with the corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal layer and the depositing is carried out to the extent of leaving no gap in each of the isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344);

planarizing with a single etch recipe the conformal layer (364) to form therefrom an upper surface for each of the isolation trench that is co-planar to the other upper surfaces, wherein:

the planarizing is performed in the absence of masking the conformal layer (364) over each of the isolation trench;

material that is electrically insulative extends continuously between and within the plurality of isolation trenches;

the conformal layer (364) and the spacers (356) form the upper surface for each isolation trench, each upper surface being formed from the conformal layer and the spacer and being situated above the pad oxide layer (340); and

the first dielectric layer (344) is in contact with at least a pair of the spacers (356) and the pad oxide layer (340). (See Figs. 2-3Q).

With respect to rounding the top edge of each isolation trench, the similar reason as that of claim 1 is also applied here.

With respect to claim 8, as best understood by the examiner, the method of Omid-Zohoor '072 further includes:

removing the pad oxide layer (340) upon a portion of the surface of semiconductor substrate (120); and

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate. (See Fig. 3P).

With respect to claim 9, 10, 12 and 13, as best understood by examiner, Omid-Zohoor '072 teaches all of the features of the claim with the exception of explicitly disclosing that the etch rate of the conformal third layer (364) and the spacers (356) being faster than that of the first dielectric layer (344).

The selectivity rate of 1:1 to about 2:1 do not appear to be critical.

The CMP process of Omid-Zohoor '072 has resulted in a planar surface (Fig. 3M). The CMP process of Omid-Zohoor '072 is stopped when the silicon nitride (344) is exposed.

Further, it appears that the etch recipe of Omid-Zohoor '072 is at least including the claimed range because the etching results in an upper surface for each the isolation trench that is co-planar to the other the upper surfaces and such selective ratios are well known. (See Fig. 3M).

Given the teaching of the reference, it would have been obvious to one having ordinary skill in the art at the time of invention to use any etch recipe which comprises a higher removal rate of the oxide than the nitride layer to form a planar surface because as the polishing reaching

the nitride layer, electrical or visual detection should be able to stop the polishing before over-etching occurred.

Within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum etch ratio of the layers. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation."

With respect to claim 11, as best understood by the examiner, the upper surface for each isolation trench (376) of Omid-Zohoor '072 is formed including:

chemical mechanical planarization, CMP, wherein the conformal layer (364), the spacers (356), and the first dielectric layer (344) form a planar first upper surface; and

an etch that forms a second upper surface, the second upper surface being situated above the pad oxide layer. (See Figs. 3A-N).

With respect to claims **18** and **24**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer;

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein the forming a second dielectric layer (352)

includes forming a second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal third layer (364), and the depositing is carried out to the extend of leaving no gap in each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344);

planarizing the conformal third layer (364) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches;

wherein planarizing the conformal third layer (364) to form therefrom the upper surface for each isolation trench that is co-planar to the other upper surface further comprises planarizing the conformal third layer (364) and each spacers (356) to form therefrom the co-planar upper

surfaces, and the planarizing the conformal third layer is performed in the absence of masking the conformal third layer (364) over each of the isolation trench; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the conformal third layer (364), and the plurality of isolation trench. (See Figs. 2-3Q).

With respect to rounding the top edge, the similar reason as that of claim 1 is also applied here.

Further, although Omid-Zohoor '072 does not explicitly disclose removing the polysilicon layer to expose the oxide layer.

However, it is within the ability of a skilled worker in the art to recognize that the polysilicon layer, formed as an alternative, also removed to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention, forming a T-shape isolation.

With respect to claim 19, as best understood by the examiner, the upper surface for each isolation trench of Omid-Zohoor '072 is formed by CMP.

With respect to claim 21, as best understood by the examiner, as taught by Omid-Zohoor '108 the liner oxide (58A) is formed upon the sidewall of the isolation trench prior to filling the isolation trench with the trench fill material (364).

Therefore, the method of Omid-Zohoor '072 in view of Omid-Zohoor '108 further includes: prior to filling each isolation trench (360) with the conformal third layer (364), forming a liner upon the sidewall of the isolation trench, the liner being confined within each isolation

trench and extending from an interface thereof with the oxide layer (340)to the termination of the isolation trench within the semiconductor substrate, and wherein the conformal third layer (364) is composed of an electrically insulative material.

With respect to claim 22, as best understood by the examiner, the liner of Omid-Zohoor '108 is a thermally grown oxide of the semiconductor substrate.

With respect to claim 23, as best understood by the examiner, forming the liner (58b) upon the sidewall of the isolation trench of Omid-Zohoor '108 comprises deposition of a composition of matter (58b).

With respect to claim **25**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer;

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein the forming a second dielectric layer (352) includes forming a second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in

contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal third layer (364), and the depositing is carried out to the extend of leaving no gap in each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344);

planarizing the conformal third layer (364) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface, wherein the planarizing the conformal third layer (364) is performed in the absence of masking the conformal third layer (364) over each of the isolation trench;

exposing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120);

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate (120);

forming in between the isolation trench, and confined in the space therebetween, a layer composed of polysilicon upon the oxide layer in contact with the pair of the spacers (356); and

selectively removing the conformal third layer (364), the spacers (356) and the layer composed of polysilicon to form a portion of at least one of the upper surfaces;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Fig. 2-3Q).

With respect to rounding the top edge, the similar reason as that of claim 1 is also applied here.

With respect to removing the polysilicon layer to expose the oxide layer, the similar reason as that of claims 18 and 24 is also applied here.

With respect to claim **26**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer;

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to exposed the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer (344), wherein the forming a second dielectric layer (352) includes forming a second dielectric layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with both polysilicon layer and the first dielectric layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal third layer (364), and the depositing is carried out to the extend of leaving no gap in each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344);

planarizing the conformal third layer (364) by an etch using an etch recipe that etches the first dielectric layer (344) slower than the conformal third layer (364) and the spacers (356) by a ratio to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface, wherein the planarizing the conformal third layer (364) is performed in the absence of masking the conformal third layer (364) over each of the isolation trench;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the conformal third layer (364) and the plurality of isolation trench. (See Figs. 2-3Q).

With respect to rounding the top edge, the similar reason as that of claim 1 is also applied here.

With respect to removing the polysilicon layer to expose the oxide layer, the similar reason as that of claims 18 and 24 is also applied here.

With respect to the etch ratio, the similar reason as that of claims 9 and 12 is also applied here.

With respect to claim 27, the similar reason as that of claims 10 and 13 is also applied here.

15. Claims **14**-17, **31**-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Poon et al. (U.S. Patent No. 5,387,540) (cited previously).

With respect to claim **14**, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a silicon nitride layer (344) upon the oxide layer (340);

selectively removing the silicon nitride layer (344) to exposed the oxide layer (340) at a plurality of areas;

forming a first silicon dioxide layer (352) over the oxide layer and the silicon nitride layer, wherein the forming of the first silicon dioxide layer (352) includes forming a first silicon dioxide layer (252) on and in contact with the exposed oxide layer (340) at the plurality of areas;

selectively removing the first silicon dioxide layer (352) to form a plurality of spacers (356) from the first silicon dioxide layer, wherein each spacer is situated upon the oxide layer

(340), is in contact with the silicon nitride layer (344), and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer (340) into and terminating within the semiconductor substrate (120), wherein each isolation trench (360) is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench has a top edge;

filling each isolation trench (360) with a conformal second silicon dioxide layer (364), the conformal second silicon dioxide layer within each isolation trench extending above the oxide layer (340) in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal second silicon dioxide layer (364), and the depositing is carried out to the extent of leaving no gap in each isolation trench and extending over the spacers (356) and the silicon nitride layer (344); and

selectively removing the conformal second silicon dioxide layer (364) and the spacers (356) to form an upper surface for each isolation trench that is co-planar to the other upper surfaces and being situated above the oxide layer (340), wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches, and wherein the selectively removing is performed in the absence of masking the conformal second dioxide layer (364) over each isolation trench. (See Figs. 2-3Q).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of explicitly forming an electrically active region below the isolation trench and

forming a liner upon the sidewall of each isolation trench and rounding the top edge of the isolation trench.

However, Poon teaches that it is well known in the art to form an electrically active region (channel stop 30) below the termination of each isolation trench to prevent the inversion. (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form an electrically active region below the termination of each isolation trench (360) of Omid-Zohoor '072 as taught by Poon to prevent the inversion.

Poon further teaches: forming a liner (28) upon a sidewall (24) of each isolation trench (22) to remove damage caused by the trench-etch.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form a liner upon a sidewall of each isolation trench (360) of Omid-Zohoor '072 as taught by Poon to remove damage caused by the trench-etch.

Note that, the formation of the thermal liner (28) is inherently result in rounding of the top edge of the isolation trench.

With respect to claim 15, as best understood by the examiner, the liner (28) of Poon is a thermally grown oxide of the semiconductor substrate.

With respect to claim 16, as best understood by the examiner, the liner of Poon is composed of silicon nitride (50).

With respect to claim 17, the process of Omid-Zohoor '072 further includes:

removing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120); and

forming a gate oxide layer (380) upon the portion of the surface of semiconductor substrate (120).

With respect to claim **31**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming a pad oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer;

forming a silicon nitride layer (344) upon the polysilicon layer;

selectively removing the silicon nitride layer (344) to exposed the pad oxide layer at a plurality of areas;

forming a first silicon dioxide layer (352) conformally over the pad oxide layer and over the silicon nitride layer (344), wherein the forming of the first silicon dioxide layer (352) includes forming the first silicon dioxide layer (352) on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the first silicon dioxide layer (352) to form a plurality of spacers (356) from the first silicon dioxide layer, wherein each spacer (356) is situated upon the pad oxide layer, is in contact with the silicon nitride layer (344) and the polysilicon layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer and from top edges into and terminating within the semiconductor substrate (120), wherein each isolation

trench is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal second layer (364), the conformal second layer extending above the pad oxide layer in contact with a corresponding pair of the spacers (356), wherein the filling is performed by depositing the conformal second layer (364), and the depositing is carried out to the extend of leaving no gap in each isolation trench (360) and extending over the spacers (356) and over the silicon nitride layer (344);

planarizing the conformal second layer (364) and each of the spacers (356) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface and is situated above the pad oxide layer (340), wherein the planarizing is performed in the absence of masking the conformal second layer (364) over each of the isolation trench;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 2-3Q).

With respect to forming of the doped region, the liner and rounding the top edge of the isolation trench, the similar reason as that of claim 14 is also applied here.

With respect to claim 32, as best understood by the examiner, the liner (28) of Poon is a thermally grown oxide of the semiconductor substrate and the conformal second layer (364) of Omid-Zohoor is composed of an electrically insulative material.

With respect to claim 33, as best understood by the examiner, the liner of Poon is composed of silicon nitride and the conformal second layer (364) of Omid-Zohoor is composed of an electrically insulative material.

With respect to claim 34, as best understood by the examiner, the method of Omid-Zohoor further comprises: (also see claim 25):

exposing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120);

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate (120);

forming in between the isolation trench, and confined in the space therebetween, a layer composed of polysilicon upon the oxide layer in contact with the pair of the spacers (356); and

selectively removing the conformal third layer (364), the spacers (356) and the layer composed of polysilicon to form a portion of at least one of the upper surfaces.

16. Claims **35**-40, **42** and **43** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Wolf *Silicon Processing for the VLSI Era*, Vol. 2, pp. 54-55.

With respect to claim 35, as best understood by the examiner, Omid-Zohoor teaches a method of forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer thereon;

forming a polysilicon layer upon the oxide layer;

forming a first layer (344) upon the polysilicon layer;

selectively removing the first layer (344) and the polysilicon layer to expose the oxide layer at a plurality areas;

forming a plurality of isolation trenches (360) through the exposed oxide layer at the plurality of areas, wherein electrically insulative material (364) extends continuously between and within the plurality of isolation trenches, each isolation trench (360):

having a spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer and the polysilicon layer;

extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the spacer;

having a second layer (364) filling the isolation trench (360) and extending above the oxide layer in contact with the spacer (356), wherein the filling is performed by depositing the second layer, and depositing is carried out to the extent of leaving no gap within each isolation trench and extending over the spacers (356) and over the first layer (344);

having a top edge; and

having a planar upper surface formed from the second layer (364) and the spacer (356) and being situated above the oxide layer, wherein the planar upper surface is formed by planarizing in the absence of masking the second layer over each of the isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the second layer (364), and the plurality of isolation trenches (360). (See Figs. 3A-M).

Thus, Omid-Zohoor is shown to teach all the features of the claim with the exception of r the top edge of the isolation trench being rounded.

However, Wolf teaches that it is well known in the art to form a rounded top edge of the isolation trench.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trench liner on the surface of trench (360) of Omid-Zohoor '072 as taught by Wolf to reduce leakage currents. Further, the rounding the top corner of the trench is an inherent result of thermally oxidizing the surface of the trench.

Further, although Omid-Zohoor does not explicitly disclose removing the polysilicon layer to expose the oxide layer.

However, it is within the ability of a skilled worker in the art to recognize that the polysilicon layer, formed as an alternative, also removed to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention.

With respect to claim 36, Wolf further teaches:

doping the semiconductor substrate with a dopant having a first conductivity type (n-type);

doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type (p-type) opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of each isolation trench. (See Fig. 2-37).

With respect to claim 37, the width of the doped trench bottom of wolf is greater than the width of the respective isolation trench.

With respect to claim **38**, as best understood by the examiner, Omid-Zohoor '072 teaches a method for forming a microelectronic structure substantially as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a first layer (344) upon the oxide layer;

selectively removing the first layer (344) to expose the oxide layer (340) at a plurality of areas;

forming a plurality of isolation trenches (360) through the oxide layer at the plurality of areas, wherein electrically insulative material (364) extends continuously between and within the plurality of isolation trench, each isolation trench (360):

having a spacer (356) composed of dielectric material upon the oxide layer (340) in contact with the first layer (344);

extending from an opening thereto at top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the spacer (356);

having a second layer (364) filling the isolation trench (360) and extending above the oxide layer (340) in contact with the spacer (356);

having a top edge; and

having a planar upper surface formed from the second layer (364) and the spacer (356) and being situated above the oxide layer (340); wherein the planar upper surface is

formed by planarizing in the absence of masking the second layer (364) over each of the isolation trench; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the second layer (364), and the plurality of isolation trenches. (See Figs. 2-3Q).

With respect to the rounded top edge of the isolation trench, a similar reason as that of claim 35 is also applied here.

With respect to claim 39, Wolf further teaches:

doping the semiconductor substrate with a dopant having a first conductivity type (n-type);

doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type (p-type) opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of isolation trenches. (See Fig. 2-37).

With respect to claim 40, the width of the doped trench bottom of wolf is greater than the width of the respective isolation trench.

With respect to claim **42**, As best understood by examiner, Omid-Zohoor '072 teaches a method for forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a polysilicon layer upon the oxide layer;

forming a first layer (344) upon the polysilicon layer;

forming a first isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344) and the polysilicon layer;

a first isolation trench (360) extending from an opening thereto at the top edges at the top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the first spacer (356), wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure having a similar structure as that of the first isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer (364), composed of an electrically insulative material, conformally filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer (340) in contact with the first and second spacers (356) of the respective first and second isolation structures (360), wherein the filling is performed by depositing the conformal second layer (364), and the depositing is carried out to the extent of

leaving no gap within each isolation trench and extending over the spaces (356) and the first layer (344); and

forming with a single etch recipe a planar upper surface from the conformal second layer (364) and the first and second spacers (356) of the respective first and second isolation structures and being situated above the oxide layer; and

wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer (364), and the first and second isolation trenches. (See Figs. 2-3Q).

With respect to the rounding of the top edges of the isolation trench and removing of the polysilicon to expose the oxide layer, a similar reason as that of claim 35 is also applied here.

With respect to claim **43**, as best understood by examiner, Omid-Zohoor teaches a method for forming a microelectronic structure substantially similar as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a first layer (344) upon the oxide layer;

forming a first isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344);

a first isolation trench (360) extending from an opening thereto at the top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the first spacer

(356), wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure having a similar structure as that of the first isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer (364), composed of an electrically insulative material, conformally filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer (340) in contact with the first and second spacers (356) of the respective first and second isolation structures, wherein the filling is performed by depositing the conformal second layer (364), and the depositing is carried out to the extent of leaving no gap within each isolation trench and extending over the spaces (356) and the first layer (344); and

planarizing the conformal second layer (364) and the first and second spacers (356) of the respective first and second isolation structures to form a planar upper surface from the conformal second layer (364) and the first and second spacers (356) of respective first and second isolation structures, and being situated above the oxide layer, wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer (364), and the first and second isolation trenches. (See Figs. 2-3Q).

With respect to the rounding of the top edges of the isolation trench, a similar reason as that of claim 35 is also applied here.

17. Claims 5 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 and Omid-Zohoor '108 as applied to claims 1 and 18 above, and further in view of Wolf or Poon '540.

Omid-Zohoor '072 and '108 teach all the features of the claim with the exception of further forming a doped region below the termination of each isolation trench.

However, Wolf or Poon teaches forming a doped region below the termination of each isolation trench to prevent inversion.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to further form a doped region below the termination of each isolation trench of Omid-Zohoor to prevent inversion.

Response to Arguments

18. Applicant's arguments filed February 14, 2002 have been fully considered but they are not persuasive.

Claim Objection:

By claiming "rounding the top edge" (claim 1) the limitation has indirectly included thermally grown oxide from the trench surface. The specification regarding "rounding of the top edge" clearly states: "[I] Fig. 5A it can be seen that, following thermal oxidation of sidewall 50

to form insulation liner 30 within isolation trench 32, semiconductor substrate 12 forms rounded edge at the top of isolation trench 32" (page 12, lines 4-6).

Therefore, the limitations: "further comprising forming a liner upon sidewall of each said isolation trench" (claim 2) and "wherein a liner is a thermally grown oxide of said semiconductor substrate" (claim 3) clearly do not further limit the subject matter has already claimed in claim 1, which these claims depend on.

The Objection therefore maintained.

Claim Rejection Under 35 U.S.C. 112, first paragraph:

Through a lengthy argument, applicant still fails to point out the specific disclosure regarding the planarizing is performed in the **absence** of masking the conformal layer, even the cited portion also fails as well.

Regarding the "single etch recipe", contrary to the applicant's conclusion, the term "the single etchbach uses an etch recipe" does not support the "single etch recipe".

Since the term "single etchbach" referring to a process, while the term "single etch recipe" (claimed term) is referring to a chemical used in the etch.

The rejections are therefore, maintained.

With respect to claim 4, 16 and 21, applicant argues that the claims recite the formation of a liner and the step of rounding the top edge of the trench as a separate limitations.

However, as clearly discloses in the specification, the liner formed by deposit, CVD, is an alternative "another method of forming insulating layer (30) is CVD" (page 12, lines 14-24).

In the specification, Applicant has recognized that forming a thermal liner results in rounded edge at the top of isolation trench 32, while deposit, CVD, does not.

Applicant fails to point out the portion of the specification that indicates rounding the corner and forming the liner is a "separate process".

Applicant further argues that :"support for this limitation can be found at page 12, line 14-16". Applicant appears to mis-interpret his own invention. The term "**Another method** of forming insulation liner is CVD" clearly shows an alternative for forming the insulation layer 30. Which means, one can have the layer 30 forms by either thermal oxidation or CVD, not both. One having ordinary skill in the art also knows that, thermal oxidation to form layer 30 also results in rounding the top edge of the trench. The layer 30, if formed by deposit, however, does not result in rounding the top edge because no silicon has been consume.

Applicant concludes that "Such a method would be understood as **including step** not expressly recited in the specification". However, the specification clearly shows an alternative, not in addition to. Since a layer forms by deposit does not inherently result in rounding the top edge, Applicant is urged to provide support for his conclusion.

The rejection is maintained.

Claim Rejection Under 35 U.S.C. 112, second paragraph:

Applicant states: "As further depicted in Figure 5-8, it can be seen that this continuous material(s) is derived from the electrically insulative materials oxide layer 14".

In response to applicant's argument that the specification show certain features of claims, it is noted that the features upon which applicant relies (i.e., wherein material that is

electronically insulative extends continuously between and within said plurality of isolation trenches) are lacking antecedent. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Reviewing the claimed terminology, one having ordinary skill in the art could not possibly know what the "material that is electronically insulative" is directed to.

The rejection is maintained.

With respect to claims 21-23, as up to the current amendment, see Paper No. 10, filed February 14, 2002, the limitation of claim 21 is: "...wherein said conformal third layer is composed of an electrically **conductive** material" (lines 5-6).

The rejection is maintained.

19. Applicant's arguments with respect to the rejection based primarily on U.S. Patent No. 6,184,108 have been considered but are moot in view of the new ground(s) of rejection.

Rejection Based PrimarilyUnder U.S. Patent No. 6,097,072

With respect to "planarizing the conformal layer ... to form therefrom an upper surface of each said isolation trench that is co-planar to the other said upper surfaces", Applicant concludes that "Accordingly, the method disclosed in the '072 patent ***does not*** planarize the conformal oxide layer 364 to produce the structure with an upper surface for each isolation trench shown in

Fig. 3M therein. Instead, the '072 patent relies upon a more complicated method with more steps".

Clearly, Applicant has recognized that '072 *does teach* planarizing the conformal layer, although relies upon a more complicated method.

Note that, the claimed limitations **do not exclude** "a more complicated method".

Additionally, Applicant also states: "In contrast, the method disclosed in the '072 patent, as previously noted, uses a multiple-step method with **different etch recipes** to form a planar upper surface".

However, '072 patent clearly discloses: "Finally, the upper surface of the oxide layer 372, along with the oxide ridge 373, is polished by chemical/mechanical polishing (CMP). A conventional CMP process is described in Silicon Processing for the VLSI Era, Volumes I, II and III by S. Wolf and R.N. Tauber" (col. 4, lines 55-60). There is no contrast between what is claimed and what is disclosed in '072 patent.

Applicant fails to point out which are the **different etch recipes** in the CMP process of '072 patent.

Applicant further adds: "claims 1, 7, 14, 18, 24-26, 31, 35, 38, and 42 recite some form of planarization that *is performed in the absence of masking of a conformal layer over at least one isolation trench*".

Note that, as discussed above, Applicant clearly tries to claim what he did not invent.

After a careful review of the present specification, one can not find support for a "planarization that *is performed in the absence of masking of a conformal layer over at least one isolation trench*".

Applicant must and should point out the support for this added limitation.

With respect to claim 34, to understand the scope of claim 34, one should review the specification with respect to "the polysilicon layer being confined in the space therebetween".

Specification, page 19, lines 6-12, discloses: polysilicon layer 24 is portion of the etch mask (see Figs. #B). Clearly, the polysilicon layer 24 forms on the oxide layer 14 is an alternative to an oxide layer 14 alone (see Fig. #A).

Note that, applicant some time refers the pad oxide as a "gate oxide": "Semiconductor substrate 12 is covered at an upper surface 42b by either a pad oxide or a gate oxide layer . Another upper surface 42c comprises the upper surface of the pad oxide or gate oxide layer". (page 18, lines 2-4). There is only one polysilicon layer (24) formed on the semiconductor substrate 12, and that polysilicon layer is formed on the pad oxide or gate oxide (as claimed).

'072 patent, clearly contemplate a similar alternative, "Also, a pad oxide containing a thin thermally-grown silicon oxide layer and a buffer polysilicon layer may be used for the pad oxide 340" (See col. 4, lines 14-16).

Since the polysilicon layer of '072 formed on the thin pad oxide layer, thus, the process disclosed by '072 clearly encompassed the limitation of claim 34. "forming between said isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon said gate oxide layer in contact with a pair of said spacers, and selectively removing said layer composed of polysilicon to form a portion of at least one of said upper surfaces".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
January 25, 2003

Wael Fahmy

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800